PENDING CLAIMS

1. (Previously presented) A clock circuit comprising:

first and second clock sources;

a multiplexer having a first input coupled to the first clock source, a second input coupled to the second clock source, and an output selectively couplable to said first and second inputs;

a clock detection circuit having an output representing a presence of said first clock source;

said multiplexer having a selection input coupled to said clock detection circuit output such that said multiplexer selects said first clock source as its output when said first clock source is present;

a phase-locked loop circuit ("PLL") having

an input coupled to said multiplexer output, and

a frequency output,

said PLL including a feedback filter circuit; and

feedforward circuitry coupled to said feedback filter circuit and to said clock detection circuit output, said feedforward circuitry selectively coupling at least one circuit element to said feedback filter circuit, wherein said selective coupling is controlled by said clock detection circuit output.

2. (Original) The circuit of claim 1, where said feedforward circuitry includes a switch controlled by said clock detection circuit output and performing said selective coupling.

3. (Original) The circuit of claim 2, wherein said switch comprises a transistor.

4. (Original) The circuit of claim 2, wherein said at least one circuit element includes a resistor.

5. (Original) The circuit of claim 4, wherein said at least one circuit element includes a capacitor in parallel with said resistor.

6. (Original) The circuit of claim 2, wherein said feedforward circuitry includes at least one of a resistor and a capacitor in parallel with said switch.

7. (Original) The circuit of claim 2, further including a bias circuit coupling said clock detection circuit output to said switch.

8. (Original) The circuit of claim 7, wherein said bias network includes a resistor based voltage divider.

9. (Original) The circuit of claim 8, further including a zener diode in parallel with at least one resistor of said resistor base voltage divider.

10. (Original) The circuit of claim 1, wherein said first clock source is received from another clock circuit within a common system.

11. (Original) The circuit of claim 10, wherein said first clock source is received over a bus.

12. (Original) The circuit of claim 11, wherein said second clock source comprises a local oscillator.

13. (Original) The circuit of claim 12, wherein said second clock source is provided to said bus.

14. (Previously presented) A system comprising:

multiple clock sources;

a switch having multiple inputs, said multiple inputs being respectively coupled to said multiple clock sources;

a clock detection circuit having an output representing a presence of one of said multiple clock sources;

said switch having a selection input coupled to said clock detection circuit output such that said switch selects one particular clock source of said multiple clock sources as its output when said one particular clock source is present;

a phase-locked loop circuit ("PLL") having

an input coupled to said switch output, and

a frequency output,

said PLL including a feedback filter circuit; and

feedforward circuitry coupled to said feedback filter circuit and to said clock detection circuit output, said feedforward circuitry selectively coupling at least one circuit element to said feedback filter circuit, wherein said selective coupling is controlled by said clock detection circuit output.

15. (Previously presented) A circuit comprising:

a clock source;

a PLL circuit having said clock source as its input;

a detection circuit coupled to said clock source and having an output representative of a presence of said clock source; and

a feedforward correction circuit coupled to said output of said detection circuit and to a feedback loop of said PLL.

16. (Previously presented) A method for controlling a clocking circuit including a clock source, the method comprising:

detecting a failure of a clock source, the clock source coupled to an input of a phase-locked loop ("PLL") circuit;

applying a control signal to said PLL in response to said failure of said clock source, said control signal altering a time constant within said PLL.

17. (Original) The method of claim 16, wherein said altering said time constant includes modifying a feedback loop within said PLL by way of said control signal.

18. (Original) The method of claim 17, wherein said altering comprises at least one of engaging and disengaging at least one circuit element into said feedback loop in response to said control signal.

19. (Original) The method of claim 16, further comprising switching another clock source to said input of said PLL in response to said control signal.

20. (Original) The method of claim 19, wherein said switching to said other clock source includes switching from a bus received clock source to a local clock source.